**CDAC Feb 2015**

Observe Setup and Hold Violations

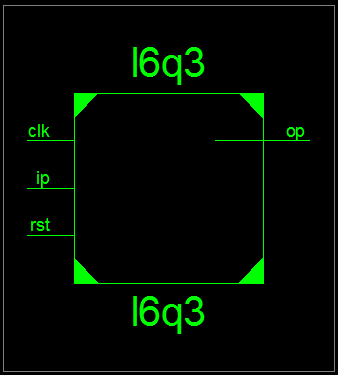
Name: Bhrigu Bhargava

**Observe Setup and Hold Violations**

# Design Approach:

To achieve the objective of analyzing the setup and hold violations, we have used a D flip flop with setup window of 3 and hold window of 4. To meet the requirement, we have to add another block called specify block which defines setup and hold time. This block can’t be written in any procedural block, it should be written separately. This will check setup for input at positive edge of clock and the setup window is 3, same as for hold window. In case of $hold first clock should be mentioned and then data should be added. Minimum time period for which there will be no setup/hold violation is found. For this. we have to take care that the first FF should be given data in such way that 1st FF do not violates.

**Block Diagram:**

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**Fig 1:- Block Diagram**

**Source Code:**

module l6q3 (output op,input ip,clk,rst);

wire opt1,opt2;

dff1 i1 (opt1,clk,rst,ip);

buf #(5) (t1,opt1);

dff2 i2 (opt2,clk,rst,t1);

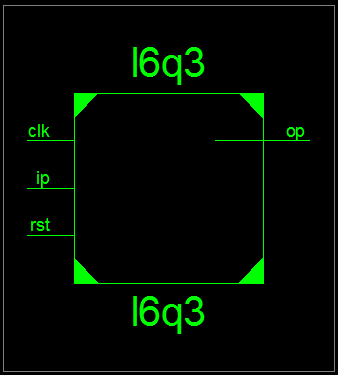
xor2 i4 (opt2,t2,t1);

dff2 i3 (op,clk,rst,t2);

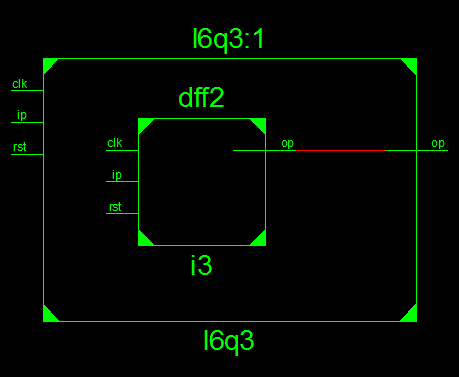
endmodule

**Synthesis:**

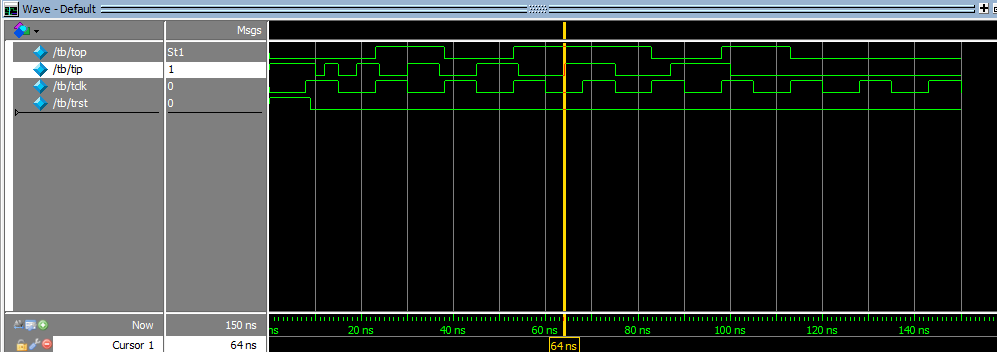
1. Block Diagram



1. RTL



1. Simulation Waveform Result

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**Error:**

None

**Verified by:**

Dharamvir Chundawat (150240133007)